REMARKS

This paper is submitted in response to the Office Action of April 17, 2007 in which claims 1-22 were rejected. With this paper, claims 1-5, 11-12 and 19-21 are amended, none are cancelled and none are added.

Claim Rejections under 35 USC §103

Claims 1-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ootani *et al* (US Patent 6,959,365, Ootani hereinafter) in view of Pline (US Publication 2004/0098545, Pline hereinafter).

Claim 1 recites a method for performing a "processing function" in a block memory. The block memory comprises memory cells for storing data and a connection bus comprising a ready/busy signal line that can be set to a ready status and to a busy status. The method comprises setting the status of the ready/busy signal line to the busy status in a beginning of the processing function, performing detection of processing errors, indicating an end of the processing function by setting the ready/busy signal line to the ready status, and, if a processing error is detected, changing the status of the ready/busy line back to the busy status.

The primary reference, Ootani, teaches a flash memory module 2 that is capable of outputting a status signal RYIBY (Fig. 1). The RYIBY signal has a ready (H) status and a busy (L) status. When an erase/write command, or a rewrite command, is accepted in the flash memory module 2 and a series of processing is being executed, the busy state (RYIBY output = L) is maintained until the series of processing has been normally completed or an error occurred. When the busy state ends, the ready state is entered (RUYIBY output =H) (col. 5, line 35-41).

As acknowledged by the Examiner, Ootani does not teach (1) performing detection of processing errors and (2) changing the status of the ready/busy line back to the busy status if a processing error is detected.

The Examiner, however, points to Pline for teaching the performing detection of processing errors (paragraph [0064]) and changing the status of the ready/busy signal line back to the busy status if a processing error is detected (paragraph [0034]).

Applicant respectfully submits that, clearly in the present invention, performing the error detection and changing the signal line back to the busy status are sequential. In Pline, however, the alleged "detecting processing errors" and "changing the status of the ready/busy signal line back to the busy status" are two separate events that are not related to each other, and the status is not "changed back" from ready to busy.

First, in paragraph [0064] (cited by the Examiner), Pline teaches detecting errors when reading out data from the memory by a so-called ECC circuit in a storage device interface (Fig. 10):

> During a data writing command, the ECC circuit 1000 receives data from the buffer 420 and adds parity bits to the data. When reading the data from the memory banks 202, the ECC circuit 1000 detects the data for errors and corrects any correctable errors in the data and then removes the parity bits and sends the corrected data back to the buffer 420 (emphasis added).

Where the ECC circuit 1000 is a part of the storage device interface 422 and the storage device interface 422 is a part of a memory controller 104 (Figs. 4A and 4B). As shown in Fig. 1, the memory controller 104 is connected to a memory 106. As the last stage of the memory controller 104, the storage device interface 422 reads data from and writes data to the memory. There is no signal line between the storage device interface 422 and the memory 106 for indicating errors in the memory (only a clock line and a data line are shown in Fig. 4B). According to Pline, the errors, if any, are detected when reading data from the memory, and they are corrected, if correctable, by the ECC circuit. Pline is silent on whether the non-correctable errors are reported to the memory controller, and there is no clear mechanism as shown in Figs. 4B and 10, nor is there any detailed description thereof in the specification, for reporting such errors.

Second, in paragraph [0034] (also cited by the Examiner), Pline teaches an additional BUSY line that is located in the interface between the memory controller 104 and the host 102:

> In addition to the DT and DR lines, a BUSY line may be added in order to provide a signal from the memory controller 104 when the memory controller 104 is busy and not ready to receive more data. The BUSY line may also be used to communicate that an error has occurred. If the fast serial transfer circuit 306 receives a BUSY signal, the transfer of data is stopped until the memory controller 104 is again ready to receive. The BUSY line remaining busy for a predetermined amount of time may be indicative of an error (emphasis added).

Therefore, the busy status may indicate either the memory controller is not ready to receive data, or an error has occurred (if the BUSY line remains busy for a predetermined amount of time). The error indication is a busy status signal and it may be the continuation of the previous busy signal that is an indication that the memory controller is not ready to receive new data. It is unlike the present invention, where a change from a ready signal back to a busy signal indicates an error has occurred.

Moreover, even if Ootani presents the utilization of ready/busy line in general for an indication of an end of process function and Pline includes details that this particular line could be utilized for error indication, neither one teaches or suggests that for optimized timing and performance, the indication of errors is given as soon as possible or necessary by changing the ready/busy line back to busy status after the a ready status indicating the process function has completed. Pline suggests that a busy signal for a longer period of time may indicate an error, such indication affects the overall timing/performance of the error indication and which is also not that practical to implement as would require usage of timers/counters which are unnecessary overheads in such an application.

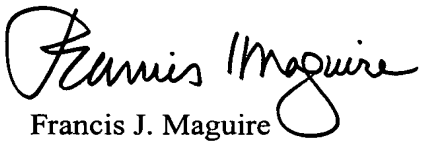
Therefore, even with Ootani and Pline combined, the present invention is not reached. It follows that Ootani and Pline are inapplicable as 35 U.S.C. Section 103(a) references against claims 1-22 and withdrawal of the obvious rejection thereof on that ground is requested.

Conclusion

For all the foregoing reasons, it is believed that all of the claims of the application are now in condition for allowance and their passage to issue is earnestly solicited.

Applicant's attorney urges the Examiner to call to discuss the present response if there are any questions.

Respectfully submitted,



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